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EXAMINER	
KITOV, ZEEV V	

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2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,189	PEZZANI, ROBERT	
	Examiner	Art Unit	
	ZEEV KITOV	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21, 23 - 39, 41 - 45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21, 23 - 39, 41 - 45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the arguments filed on October 14, 2008. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 26 and 41 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shinoda (US 4779036). Regarding claims 1, 26 and 41, Shinoda discloses both a switch and a method for controlling an SCR-type switch (Fig. 5 elements 70a-f), comprising applying on the switch gate several periods of an unrectified high frequency voltage (col. 5 lines 11-17 & Fig. 8F). Shinoda discloses that in normal, i.e. non-ideal environmental conditions, there is no guarantee that a single pulse provided to the gate will fire the SCR (col. 5, line 60 – col. 6, line 2), which is an evidence that the power of

each half-wave of the unrectified high frequency voltage is insufficient to start the SCR-type switch. As a result, as shown in Fig. 8F, plural half periods of a high frequency signal are supplied to the gate, thus causing a gradual increase of the gate potential over time, to start the SCR. As to accumulated effect of the successive high frequency AC signal on the SCR's gate, it is inherent in the structure and principle of action of the SCR. It is because of presence of an emitter-base junction capacitance, which accumulates the charges thus giving a rise to an accumulated base-emitter potential. An evidence of inherency is provided by Boylestad et al. textbook Electronic Devices and Circuit Theory describing the semiconductor junction capacitance as being dependent on a value of an applied voltage (Fig. 1.33). According to Boylestad et al., with a forward (positive) bias the junction has a substantial value of a diffusion capacitance while with a reverse (negative) bias it has much smaller value of a depletion capacitance. Since the capacitance is non-linear and dependent on a value of an applied signal, the junction is capable of accumulating predominantly positive charges due to its larger capacitance and therefore larger charge storage capability. One of ordinary skill in the art would recognize that such accumulation of charges in the emitter-base junction of the SCR transistor makes possible firing the SCR by applying several periods of the high frequency wave while individual half way is not sufficient to fire it. When a bipolar wave of the high frequency signal becomes DC biased due to accumulation of positive charges in the emitter-base junction of the SCR, a peak value of the signal wave rises higher. Therefore, for the high frequency signal being barely sufficient for triggering the SCR due to its accumulated DC bias, such as taught by

Shinoda, its half period value alone (without DC bias) would not be sufficient for triggering.

As an additional evidence of the presence of emitter-base junction capacitances the examiner provides the following US patents: Dumont et al. (US 4,459,531), (col. 4 line 61 to col. 5 line 15), Yakushi et al. (US 4,982,259), col. 1 lines 31-38) and Croft (US 5,546,038, col. 4 lines 46-58, Figs. 1A-1C). Such capacitance is especially evident in the isolated gate devices such as isolated gate thyristor of Iwamuro et al. discussed further in the Office Action. According to Iwamuro et al. (col. 17, lines 31 – 41), "the gate capacity (capacitance) was reduced due to the increase in the thickness of the gate oxide film".

Regarding Claim 41, the high frequency signal is inherently supplied to the control electrode "close enough in time".

Regarding claims 2 and 42, Shinoda discloses the method of claim 1, wherein the high frequency voltage oscillates at a selected frequency between 10 kHz and a few GHz, i.e. at 20 Khz (col. 5 lines 67-68).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Shinoda in view of Iwamuro et al. and Hui et al. article Coreless transformers for Power MOSFET/IGBT Gate Drive Circuits. Regarding these Claims, Shinoda although discloses the high frequencies but does not disclose frequencies in megahertz region. Hui et al. disclose that substantially simpler and cheaper structure of an isolation transformer for driving power semiconductors may be achieved by using PCB technology, which is possible only when using high enough frequencies, such as ranging from 500 Khz to 2 Mhz (see Abstract). It would have been obvious to one having ordinary skills in the art at the time the invention was made to increase the workable range from single and tens of KHz (Shinoda) to 1 MHz or higher, because according to Hui et al. article it would considerably simplify a structure of the coupling transformer, which may be built in a form of printed traces on the top of PCB without using ferromagnetic core.

Claims 7, 25, 44 and 45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shinoda in view of Nuckolls (US 3344310). Regarding claims 7 and 25, Shinoda discloses driving the SCR by application of the high frequency voltage wave at a selected frequency between 10 kHz and a few GHz (col. 5 lines 67-68). However, Shinoda discloses delivering the pulses to the SCR's gate through isolating transformers (69a - 69c in Fig. 6), which satisfies the limitations of claim 7, but does not satisfies the limitation of claim 25, requiring delivering the pulses through capacitors.

Nuckolls discloses a method of controlling an SCR-type switch (Fig. 1), the method comprising: providing a control signal to a gate of the SCR-type switch (7 and 8) that controls the SCR-type wherein the control signal is provided to the gate through a capacitor (56 and 57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Shinoda system by replacing the isolating transformers by capacitors according to teachings of Nuckolls, because in conditions when isolation from the ground is not required, delivering the pulses from the oscillator to the SCR's gate through capacitor would be a simple substitution of one known equivalent element for another and substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art. *In re Fout,* 675 F.2d 297, 213 USPQ 532 (CCPA 1982).

Regarding Claim 44 and 45, Shinoda discloses providing to the gate of the SCR a plurality of half-ways of the high frequency voltage in succession turning on the SCR switch (Fig. 8F). As to creating accumulating effect in the SCR, this issue was addressed in Claim 1 rejection (see above).

Claims 3 – 24 and 43 are rejected under 35 U.S.C.§103(a) as being unpatentable over Shinoda (US 4779036) in view of Iwamuro et al. (US 6,091,087).

Regarding claims 8 and 13 Shinoda discloses an SCR-type switch component (70a- 70f in Fig. 5), comprising two main electrodes (anodes and cathodes of elements 70a-f in Fig. 5) and at least one control electrode (Fig. 5 gates of elements 70a-f) controlling the SCR-type switch component in response to an unrectified high frequency power supply

(col. 5 lines 11-17 and Fig. 8F frequency burst to provide sufficient energy to start the SCR-type switch).

Shinoda does not specifically disclose that the SCR-type switch component with the gate formed on an insulating layer that insulates the control electrode from a starting region of the component (for claim 8) and Shinoda does not specifically disclose that the control of the SCR-type switch controls without supplying current from the control terminal to the starting area of the SCR-type switch (for claims 3 and 13).

Regarding claims 8, 13 and 43, Iwamuro et al. teaches an insulated gate thyristor (Fig. 1), which has the gate electrode (10 in Fig. 1) formed on an insulating layer that insulates the control electrode from a starting region of the component (area below the gate in Fig. 1). Due to this insulation the gate does not conduct the current to the starting region of the component.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda device with the insulated gate thyristor of Iwamuro et al. because using these devices of Iwamuro et al. greatly contributes to reduction of switching losses in a power switching apparatus.

Regarding claims 4 and 9 Shinoda in view of Iwamuro et al. discloses the SCR-type switch component of claim 8. Iwamuro et al. further discloses the control electrode (10 in Fig. 1) being arranged above a gate region of a thyristor (9 in Fig. 1).

Regarding Claims 7, 12 and 24, Shinoda disclose the high frequency pulses being applied through the winding of the transformers (69a, 69b and 69c in Fig. 6) inherently generating a magnetic fields.

Regarding claims 5 and 10 Shinoda in view of Iwamuro et al. discloses the SCR-type switch component of claim 8, but does not disclose the control electrode being arranged above a gate region of a triac. Iwamuro et al. disclose arranging the control electrode of the thyristor above its gate region, i.e. above a channel region right below the gate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda SCR device by arranging the control electrode above the gate region of triac, i.e. a channel region right below the gate, in a way similar to Iwamuro et al. because the thyristor provides only unidirectional conduction and a triac would provide bidirectional conduction and therefore can be used for switching both polarities of the AC voltage by a single device. Note that a triac is a configuration of a pair of thyristors connected in anti-parallel manner. Such modification would allow use of a single switching device (triac) rather than two SCR's, as Shinoda teaches. In Shinoda circuit such modification would allow substantial reduction of parts count, not only of the SCR's, but also reduction of count of the gate isolating transformers.

Regarding claims 6 and 11 Shinoda in view of Iwamuro et al. discloses the SCR-type switch component of claim 8.

Shinoda further teaches the control electrode being a high-frequency line having terminals for connection to the high frequency power supply (col. 6 lines 7-13 and Fig. 5 elements 70 a-f).

Regarding claims 14 and 15, Shinoda in view of Iwamuro et al. discloses the SCR-type switch component of claim 13. Shinoda further discloses wherein the high frequency

voltage oscillates at a selected frequency between 10 kHz and a few GHz, i.e. at 20 Khz (col. 5 lines 67-68), i.e. at frequencies higher than 1 Mhz.

Regarding claim 17 Shinoda in view of Iwamuro et al. discloses the method of claim 13. Iwamuro et al. further teaches the control terminal (gate electrode) being insulated from the starting area, i.e. the channel just below the gate area (Fig. 1 elements 9 and 10).

Regarding claims 18 - 21 Shinoda in view of Iwamuro et al. discloses the method of claims above. Shinoda further teaches the high-frequency control voltage comprising a plurality of halfwaves, wherein each one of the plurality of halfwaves is individually insufficient to turn on the SCR-type switch since the charge the half way pulse carries is insufficient for starting the SCR conduction (see Claim 1 rejection above).

Regarding claim 23 Shinoda in view of Iwamuro et al. discloses the method of claim 13. Shinoda further discloses wherein the high-frequency control voltage is unrectified (Fig. 8F).

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Shinoda (US 4779036) in view of Iwamuro et al. (US 6091087) and J. A. Nuckolls (US 3344310).

Regarding claim 16 Shinoda in view of Iwamuro et al. discloses the method of claim 13 but does not teach wherein the high frequency control voltage is provided to the control terminal through a capacitor. Nuckolls teaches controlling an SCR-type switch (Fig. 1 elements 7 & 8) wherein the high frequency control voltage is provided to the control terminal through a capacitor (Fig. 1 elements 56 & 57). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the

Shinoda in view of Iwamuro et al. device with the capacitor of Nuckolls because it provides isolation from the circuit by providing AC coupling.

Claims 27, 28 and 33 - 43 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shinoda (US 4779036) in view of Bhagat (US 4630092).

Regarding claims 27 and 28, Shinoda discloses an SCR-type switch component (elements 70a-f in Fig. 5), comprising two main electrodes (anodes and cathodes of elements 70a-f in Fig. 5) and at least one control electrode (terminals 7b and 7d in Fig. 5) controlling the SCR-type switch component in response to an unrectified high frequency power supply (col. 5, lines 11-17 and Fig. 8F teach providing sufficient energy to start the SCR-type switch). As to response to accumulated effect of a plurality of halfwaves, the issue was fully addressed in Claim 1 rejection. However, Shinoda does not disclose a structure of the SCR device including the starting region and insulating region.

Bhagat teaches a starting region (elements 22, 24 and 30, 38 in Fig. 2) and insulating region (elements 40, 46 in Fig. 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda device by introducing the completely insulated gate thyristor of Bhagat because this thyristor with insulated gate provides rapid turn-off even when anode voltage stays high (Bhagat).

Regarding claim 28, Bhagat further discloses the first control electrode (gate) being completely insulated from the starting region (elements 42, 40, 46 in Fig. 2).

Regarding claim 33 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Bhagat further discloses the first control electrode being insulated, via the insulating layer, from a semiconductor substrate in which semiconductor layers of the SCR-type switch component are formed (Fig. 2).

Regarding claim 34 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Bhagat further discloses a second control electrode being insulated from the starting region by the insulating region (Fig. 2 elements 42, 40, 46).

Regarding claim 35 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Bhagat further discloses wherein the starting region comprises a first region of a first conductivity type (element N- in Fig. 2) and a second region of a second conductivity type (element P- in Fig. 2), wherein the first control electrode is closer to the first region than to the second region (element 44, N in Fig. 2), and wherein the second control electrode is closer to the second region than to the first region (element 42, PN in Fig. 2).

Regarding claim 36 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Bhagat further discloses wherein the first control electrode contacts the insulating region (elements 44, 40, 46 in Fig. 2).

Regarding claim 37 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Bhagat further discloses wherein the insulating region contacts the starting region (elements 40, N in Fig. 2).

Regarding claim 38 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27 but does not disclose wherein the control electrode is arranged above a gate region

of a triac. Note that a triac is a configuration of a pair of thyristor connected back to back. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda in view of Bhagat device with a triac because a thyristor provides only unidirectional rectification and a triac would provide bidirectional rectification. Such modification would allow use of a single switching device (triac) rather than two SCR's as Shinoda uses. In Shinoda circuit such modification would allow substantial reduction of parts count, not only of the SCR's, but also reduction of count of the gate isolating transformers.

Regarding claim 39 Shinoda in view of Bhagat discloses the SCR-type switch of claim 27. Shinoda further teaches wherein the SCR-type switch is a thyristor (elements 70a-f in Fig. 5).

Regarding claim 41 Shinoda in view of Bhagat discloses the SCR-type switch of claim 40. Shinoda further teaches wherein the SCR-type switch is only turned on in response to a combined effect of a plurality of halfwaves of the high-frequency control voltage but is not turned on in response to an effect of an individual one of the plurality of halfwaves (Fig. 8F shows a frequency burst or plurality of halfwaves to provide sufficient energy to start the SCR-type switch).

Regarding claim 42 Shinoda in view of Bhagat discloses the SCR-type switch of claim 40 except for the range of 1 MHz or higher. It would have been obvious to one having ordinary skills in the art at the time the invention was made to increase the workable range from 10 KHz to 1 MHz or higher, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable

ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 43 Shinoda in view of Bhagat discloses the SCR-type switch of claim 40.

Bhagat further teaches wherein the high-frequency control voltage controls the SCR-type switch without supplying current from the control terminal to the starting area (Fig. 2 elements 40, 46).

Claim 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shinoda (US 4,779,036) in view of Bhagat (US 4,630,092) and Spink (US 3,824,444).

Regarding claim 29 Shinoda in view of Bhagat disclose the SCR-type switch method of claim 27. Shinoda in view of Bhagat does not disclose wherein the control electrode is inductively coupled to the starting region via the insulating region. Spink teaches wherein the control electrode is inductively coupled to the starting region via the insulating region (Fig. 1 elements GT1, GT2, GT3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda in view of Bhagat device with the winding of Spink to provide better isolation for the control gate of the semiconductor. Such arrangement besides isolation makes the gate electrode and starting structure being totally independent from the grounding problem for the starting signal.

Claims 30-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Shinoda (US 4779036) in view of Bhagat (US 4630092) and J. A. Nuckolls (US 3344310).

Regarding claim 30 Shinoda in view of Bhagat discloses the SCR-type switch method of claim 27. Shinoda in view of Bhagat does not disclose wherein the first control electrode is capacitively coupled to the starting region via the insulating region. J. A. Nuckolls teaches disclose wherein the first control electrode is capacitively coupled to the starting region via the insulating region (Fig. 1 element 56). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Shinoda in view of Bhagat device with the capacitor of J. A. Nuckolls because it provides isolation from the circuit by providing AC coupling.

Regarding claim 31 Shinoda in view of Bhagat and J. A. Nuckolls discloses the SCR-type switch method of claim 30. Bhagat further teaches the first control electrode contacting the insulating region (Fig. 2 elements 44, 40).

Regarding claim 32 Shinoda in view of Bhagat and J. A. Nuckolls discloses the SCR-type switch method of claim 31. Bhagat further teaches wherein the insulating region contacts the starting region (Fig. 2 elements 40, 32, 34, 36).

Response to Arguments

Applicant's arguments filed on July 21, 2008 have been fully considered but they are not persuasive. Examiner chose to answer this response rather than the later response filed on October 14, 2008, since due to a change of the grounds of rejection the prior response is the most adequate.

Applicant attacks the Shinoda reference used in the current version of the rejection alleging that "Shinoda switch does not turn on in response to accumulated

effect" (page 9 bottom paragraph). However, Shinoda discloses that in normal, i.e. non-ideal environmental conditions, there is no guarantee that a single pulse provided to the gate will fire the SCR (col. 5, line 60 – col. 6, line 2), which is an evidence that the power of each half-wave of the unrectified high frequency voltage is insufficient to start the SCR-type switch. As a result, as shown in Fig. 8F, plural half periods of a high frequency signal are supplied to the gate, thus causing a gradual increase of the gate potential over time, i.e. accumulated effect, to start the SCR. As to the accumulated effect of the successive high frequency AC signal on the SCR's gate, it is inherent in the structure and principle of action of the SCR. It is because of presence of an emitter-base junction capacitance, which accumulates the charges thus giving a rise to an accumulated base-emitter potential. An evidence of inherency is provided by Boylestad et al. textbook Electronic Devices and Circuit Theory describing the semiconductor junction capacitance as being dependent on a value of an applied voltage (Fig. 1.33). According to Boylestad et al., with a forward (positive) bias the junction has a substantial value of a diffusion capacitance while with a reverse (negative) bias it has much smaller value of a depletion capacitance. Since the capacitance is non-linear and dependent on a value of an applied signal, the junction is capable of accumulating predominantly positive charges due to its larger capacitance and therefore larger charge storage capability. Such accumulation of charges in the emitter-base junction of the SCR transistor makes possible firing the SCR by applying several periods of the high frequency wave while individual half way is not sufficient to fire it. When a bipolar wave of the high frequency signal becomes DC biased due to accumulation of positive

charges in the emitter-base junction of the SCR, a peak value of the signal wave rises higher. Therefore, for the high frequency signal being barely sufficient for triggering the SCR due to its accumulated DC bias, its half period value alone (without DC bias) would not be sufficient for triggering.

Applicant further attacks the Shinoda reference for not explicitly stating a presence of parasitic capacitance. However, as stated in the Office Action, the input capacitance is an inherent feature of the of the SCR device. The Office Action further bring following evidence of such inherency: "as an additional evidence of the presence of emitter-base junction capacitances the examiner provides the following US patents: Dumont et al. (US 4,459,531), (col. 4 line 61 to col. 5 line 15), Yakushi et al. (US 4,982,259), col. 1 lines 31-38) and Croft (US 5,546,038, col. 4 lines 46-58, Figs. 1A-1C). Such capacitance is especially evident in the isolated gate devices such as isolated gate thyristor of Iwamuro et al. discussed further in the Office Action. According to Iwamuro et al. (col. 17, lines 31 – 41), "the gate capacity (capacitance) was reduced due to the increase in the thickness of the gate oxide film" ".

Applicant further alleges: "The Officer Action has provided no rationale as to how the presence of parasitic capacitance implies the creation of an accumulated effect b y applying the several periods in succession" (page 10, 2nd paragraph). However, the recited above passage from the Office Action speaks for itself. The accumulated effect across the parasitic capacitance in the gate of the SCR is provided with well based

explanation (see above). Therefore the Applicant's conclusion that it is legally insufficient is baseless.

As to Applicant's attack on the Shinoda reference for allegedly not disclosing: "the power of each half way ... is individually insufficient to start the switch" However, as stated in the Office Action, Shinoda discloses that in normal, i.e. non-ideal environmental conditions, there is no guarantee that a single pulse provided to the gate will fire the SCR (col. 5, line 60 – col. 6, line 2), which is an evidence that the power of each half-wave of the unrectified high frequency voltage is insufficient to start the SCR-type switch.

Applicant further attacks the Shinoda reference alleging that even with accumulated effect the SCR may be not ignited (started) (page 10, bottom paragraph - page 11, 1st paragraph). However, assuming, for the sake of argument only) that the Applicant's argument is true, then the Shinoda SCR would not start in any conditions, including non-ideal environmental conditions, presenting a problem for firing the SCR. Therefore, the Applicant's criticism is non-convincing.

Examiner believes that the recited part of Claim 1 rejection provides an adequate response to any criticism of Shinoda reference.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272- 2052. The examiner can normally be reached on Mon- Fri from 8:30 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.
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/Z. K./
Examiner, Art Unit 2836
11/3/2008
/Stephen W Jackson/
Primary Examiner, Art Unit 2836